



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : William R. Wheeler et al.  
Serial No.: 09/941,952  
Filed : August 29, 2001  
Assignee : Intel Corporation  
Title : SIMULATING A LOGIC DESIGN

Art Unit: 2123  
Examiner:

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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Office action on the merits. No fee is required.

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Applicant : William R. Wheeler et al.  
Serial No.: 09/941,952  
Filed : August 29, 2001


Attorney's Docket No.:10559-597001

Examiner's initials in the left column per MPEP 609 are  
earnestly solicited along with an early action on the merits.

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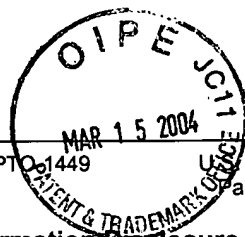
Respectfully submitted,

Date: 3/12/04

  
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Substitute Form PTO-1449 (Modified)  <b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-597001	Application No. 09/941,952
	Applicant William R. Wheeler et al.		
	Filing Date August 29, 2001	Group Art Unit 2123	

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	RE 38,059	04/2003	Yano, et al.			
	AB	4,703,435	10/1987	Darringer, et al.			
	AC	4,970,664	11/1990	Kaiser, et al.			
	AD	5,212,650	05/1993	Hooper, et al.			
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	AAA	5,831,869	11/1998	Ellis, et al.			

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ABB	5,841,663	11/1998	Sharma, et al.			
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	ADD	5,903,469	05/1999	Ho			
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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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### Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
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	AWWW	08-314892	11/1996	Japan				
	AXXX	2001-068994	03/2001	Japan				
	AYYY	WO 98/37475	08/1998	WIPO				
	AZZZ	WO 98/55879	12/1998	WIPO				

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**Foreign Patent Documents or Published Foreign Patent Applications**

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							Yes	No
Q	AAAAA	WO 99/39268	08/1999	WIPO				
"	ABBBB	WO 00/65492	11/2000	WIPO				

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	ADDDD	Kutzschebauch, "Efficient logic optimization using regularity extraction", Proceedings of 2000 International Conference on Computer Design, September 17, 2000, pp. 487-493.
	AEEEE	Lahti, et al., "SADE: a Graphical Toll for VHDL-Based System Analysis", 1991 IEEE International Conference on Computer-Aided Design, November 11, 1991, pp. 262-265.
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	AGGGG	NB84035598, "Binary Relational Schema to Model Structured LSI Design", IBM Technical Disclosure Bulletin, Vol. 26, No. 10B, March 1984, pp. 5598-5601.
	AHHHH	NN7807629, "Functional Oriented Symbolic Macromodeling Algorithm", IBM Technical Disclosure Bulletin, Vol. 21, No. 2, July 1978, pp. 629-631.
	AIIII	NN8006341, "Macro Physical-To-Logical Checking LSI Chip Design", IBM Technical Disclosure Bulletin, Vol. 23, No. 1, June 1980, pp. 341-345.
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	ALLLL	Su, Stephen, "An Interactive Design Automation System", <i>Proceedings of the 10th Design Automation Workshop on Design Automation</i> , pp. 253-261, June 1973
"	AMMMM	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

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